**Amendments to the Claims**

This listing of the claims replaces all previous listings and versions of the claims.

Listing of the Claims

1-22. (canceled)

23. (previously presented) A semiconductor integrated circuit device comprising:

a first conductivity type substrate;

MOS transistors disposed in said substrate and including first insulating films; and

an MOS type varactor element disposed in said substrate and including a second insulating film, a conductive electrode and a second conductivity type well,

wherein said second insulating film, said conductive electrode and said second conductivity type well form a variable capacitor,

wherein said first insulating films have a plurality of different thicknesses,

wherein a thickness of said second insulating film is thinner than that of the thinnest insulating film among said first insulating films of said MOS transistors, and

wherein first and second diffusion layers are provided at both sides of said conductive electrode, and said first and

second diffusion layers are connected to a common terminal through first and second wiring line respectively.

24. (previously presented) The semiconductor integrated circuit device according to claim 23, wherein a variable capacitance is formed between said conductive electrode and said second conductivity type well, and said variable capacitance is response to a voltage between said conductive electrode and said second conductivity type well.

25. (previously presented) The semiconductor integrated circuit device according to claim 23, wherein maximum gate voltage applied to said MOS type varactor element is lower than a minimum gate voltage applied to said MOS transistors.

26. (previously presented) The semiconductor integrated circuit device according to claim 23, wherein said MOS transistors include an N-channel MOS transistor and P-channel MOS transistor.

27. (previously presented) The semiconductor integrated circuit device according to claim 23, wherein said first and second diffusion layers are second conductivity type diffusion layers.

28. (previously presented) The semiconductor integrated circuit device according to claim 27, wherein said common terminal supplies with a potential of said second conductivity type well through said first and second diffusion layers.

29. (previously presented) The semiconductor integrated circuit device according to claim 23, wherein said first and second diffusion layers are first conductivity type diffusion layers.

30. (previously presented) The semiconductor integrated circuit device according to claim 29, wherein said MOS type varactor element further comprises a third diffusion layer disposed in said second conductivity type well, said third diffusion layer is connected to a terminal different from said common terminal through a third wiring line.

31. (previously presented) The semiconductor integrated circuit device according to claim 30, wherein said third diffusion layer is a second conductivity type diffusion layer.

32. (previously presented) The semiconductor integrated circuit device according to claim 31, wherein said terminal supplies with a potential of said second conductivity type well through said third diffusion layer.

33. (previously presented) The semiconductor integrated circuit device according to claim 32, wherein said common terminal supplies said first and second diffusion layers with a ground potential.

34. (previously presented) The semiconductor integrated circuit device according to claim 23, wherein a thickness of said second insulating film of said MOS type varactor element is about

three quarters of a thickness of first insulating films of said MOS transistors.

35. (previously presented) The semiconductor integrated circuit device according to claim 34, wherein the thickness of said second insulating film of said MOS type varactor element is about 6 nm.

36. (previously presented) A semiconductor integrated circuit device comprising:

a first conductivity type substrate;

MOS transistors disposed in said substrate and including first insulating films; and

an MOS type varactor element disposed in said substrate and including a second insulating film, a conductive electrode and a second conductivity type well,

wherein said second insulating film, said conductive electrode and said second conductivity type well form a variable capacitor,

wherein said first insulating films all have a same thickness,

wherein a thickness of said second insulating film is thinner than the same thickness of said first insulating films of said MOS transistors, and

wherein first and second diffusion layers are provided at both sides of said conductive electrode, and said first and

second diffusion layers are connected to a common terminal through first and second wiring lines respectively.

37. (previously presented) The semiconductor integrated circuit device according to claim 36, wherein a variable capacitance is formed between said conductive electrode and said second conductivity type well, and said variable capacitance is response to a voltage between said conductive electrode and said second conductivity type well.

38. (previously presented) The semiconductor integrated circuit device according to claim 36, wherein maximum gate voltage applied to said MOS type varactor element is lower than a minimum gate voltage applied to said MOS transistors.

39. (previously presented) The semiconductor integrated circuit device according to claim 36, wherein said MOS transistors include an N-channel MOS transistor and P-channel MOS transistor.

40. (previously presented) The semiconductor integrated circuit device according to claim 36, wherein said first and second diffusion layers are second conductivity type diffusion layers.

41. (previously presented) The semiconductor integrated circuit device according to claim 40, wherein said common terminal supplies with a potential of said second conductivity type well through said first and second diffusion layers.

42. (previously presented) The semiconductor integrated circuit device according to claim 36, wherein said first and second diffusion layers are first conductivity type diffusion layers.

43. (previously presented) The semiconductor integrated circuit device according to claim 42, wherein said MOS type varactor element further comprises a third diffusion layer disposed in said second conductivity type well, said third diffusion layer is connected to a terminal different from said common terminal through a third wiring line.

44. (previously presented) The semiconductor integrated circuit device according to claim 43, wherein said third diffusion layer is a second conductivity type diffusion layer.

45. (previously presented) The semiconductor integrated circuit device according to claim 44, wherein said terminal supplies with a potential of said second conductivity type well through said third diffusion layer.

46. (previously presented) The semiconductor integrated circuit device according to claim 45, wherein said common terminal supplies said first and second diffusion layers with a ground potential.

47. (previously presented) The semiconductor integrated circuit device according to claim 36, wherein a thickness of said second insulating film of said MOS type varactor element is about

three quarters of a thickness of first insulating films of said MOS transistors.

48. (previously presented) The semiconductor integrated circuit device according to claim 47, wherein the thickness of said second insulating film of said MOS type varactor element is about 6 nm and the thickness of first insulating films of said MOS transistors is about 8 nm.

49. (new) The semiconductor integrated circuit device according to claim 23, wherein said MOS type varactor element has only one insulating film as a capacitor insulating film, the only one insulating film being said second insulating film.

50. (new) The semiconductor integrated circuit device according to claim 36, wherein said MOS type varactor element has only one insulating film as a capacitor insulating film, the only one insulating film being said second insulating film.